REMARKS

Applicants acknowledge the Examiner's indication that claims 6 and 8 define patentable subject matter and that these claims would be allowed if rewritten in independent form including all limitations of the base claim from which they depend and any intervening claims.

Applicants respectfully request that the Examiner acknowledge Applicants' priority claim, and the receipt of the certified copy of the Korean priority document.

Applicants hereby amend claims 1-3, 5, 6, 9, 10 and 11. Accordingly, claims 1-11 remain pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following remarks.

OBJECTION TO SPECIFICATION

Applicants thank the Examiner for providing information about recommended section headings. However, Applicants respectfully decline to amend the headings. Section headings are not statutorily required for filing a non-provisional patent application under 35 USC 111(a), but per 37 CFR 1.51(d) are only guidelines that are suggested for applicant's use. (See Miscellaneous Changes in Patent Practice, Response to comments 17 and 18 (Official Gazette, August 13, 1996) [Docket No: 950620162-6014-02] RIN 0651-AA75 ("Section 1.77 is permissive rather than

mandatory. ... [T]he Office will not require any application to comply with the format set forth in 1.77").

35 U.S.C. § 102 and 103

The Office Action rejects claims 1-5 and 9-11 under 35 U.S.C. § 102 over Applicants' Admitted Prior Art ("AAPA"), and claim 7 under 35 U.S.C. § 103 over AAPA in view of Kawamura U.S. Patent 5,485,424 ("Kawamura").

Applicants respectfully submit that all of the claims 1-5, 7 and 9-11 are patentable under 35 U.S.C. § 102 and 103 for at least the following reasons.

Claim 1

Among other things, the device of claim 1 includes a data converter which sequentially outputs amplified N bits of data from each of the memory array blocks, beginning with the amplified N bits of data from a memory array block nearest to the RAS chain and subsequently outputting the amplified N bits of data from a memory array block farthest from the RAS chain.

The AAPA, and particularly the device of FIG. 4, includes no such feature.

Accordingly, for at least this reason, Applicants respectfully submit that claim 1 is patentable over the AAPA.

Claims 2-5 and 9

Claims 2-5 and 9 depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 5

Claim 5 has been rewritten in independent form without any other changes, and therefore is of identical scope to the originally filed claim 5.

Among other things, in the device of claim 5, the nearer a memory array block comes to the RAS chain, the greater the number of the memory sub-blocks of the memory array block. An exemplary embodiment illustrating such a feature is shown in FIG. 6.

The Office Action states that the AAPA discloses such a feature, citing FIG. 4.

Applicants respectfully disagrees. Indeed, in FIG. 4, each of the shown eight memory array blocks has an identical number (three) of memory sub-blocks.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 5 is patentable over the AAPA.

Claim 9

Among other things, in the device of claim 9, the memory array block closest to the RAS chain has a greater number of the memory sub-blocks than the memory array block farthest from the RAS chain.

Applicants respectfully submit that the AAPA discloses no such feature. Indeed, each of the shown eight memory array blocks shown in FIG. 4 has an identical number (three) of memory sub-blocks.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 9 is patentable over the AAPA.

Claim 7

Claim 7 depends from claim 1. Applicants respectfully submit that Kawamura does not remedy the shortcomings of the AAPA as set forth above with respect to claim 1.

Accordingly, Applicants respectfully submit that claim 7 is patentable over any possible combination of the AAPA and Kawamura.

Claim 10

Among other things, in the device of claim 10, the nearer a memory array block is to the RAS chain, the smaller the number of the memory sub-blocks of the memory array block. An exemplary embodiment illustrating such a feature is shown in FIG. 8.

The Office Action states that the AAPA discloses such a feature, citing FIG. 4.

Applicants respectfully disagrees. Indeed, in FIG. 4, each of the shown eight memory array blocks has an identical number (three) of memory sub-blocks.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 10 is patentable over the AAPA.

Claim 11

Claim 11 depends from claim 10 and is deemed patentable for at least the reason set forth above with respect to claim 10.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1-11, and

pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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Date: 27 October 2004 By: _____
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